

 **M-TECH VLSI PROJECTS LIST (2019-20)**

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| **S.NO** | **PROJECT TITLE** | **YEAR** | **DESIGN** |
|  | A Decoder for Short BCH Codes With High Decoding Efficiency and Low Power for Emerging Memories | 2019 | Front End |
|  | Approximate Reverse Carry Propagate Adder for Energy-Efficient DSP Applications | 2019 | Front End |
|  | Architecture Optimization and Performance Comparison of Nonce-Misuse-Resistant Authenticated Encryption Algorithms | 2019 | Front End |
|  | TOSAM:AnEnergy-EfficientTruncation-andRounding-BasedScalableApproximate Multiplier | 2019 | Front End |
|  | Design And Analysis Of Approximate Redundant Binary Multipliers.  | 2019 | Front end |
|  | Rounding Technique Analysis Of Power-Area & Energy Efficient Approximate Multiplier Design  | 2019 | Front end |
|  | A Combined Arithmetic-High-Level Synthesis Solution to Deploy Partial Carry-Save Radix-8 Booth Multipliers in Datapath. | 2019 | Front end |
|  | Low Power High Accuracy Approximate Multiplier Using Approximate High Order Compressors. | 2019 | Front end |
|  | Efficient Modular Adder Designs Based on Thermometer & One-Hot Encoding | 2019 | Front End |
|  | Error Detection And Correction In SRAM Emulated TCAMs | 2019 | Front end |
|  | Efficient Design For Fixed Width Adder Tree  | 2019 | Front end |
|  | Area –Time Efficient Streaming Architecture For Architecture For FAST And BRIEF Detector | 2019 | Front end |
|  | Hard Ware Efficient Post Processing Architecture For True Random Number Generators | 2019 | Front end |
|  | A Two Speed Radix -4 Serial –Parallel Multiplier | 2019 | Front end |
|  | Low power approximate unsigned multipliers with configurable error recovery | 2019 | Front end |
|  | Energy Quality Scalable Adders Based On Non Zeroing Bit Truncation | 2019 | Front end |
|  | Double MAC On A DSP Boosting The Performance Of Convolutional Neural Networks On FPGAS | 2019 | Front end |
|  | A Low-Power Parallel Architecture for Linear Feedback Shift Registers | 2019 | Front end |
|  | Ultra-low-voltage GDI-based hybrid full adder design for area and energy-efficient computing systems | 2019 | BACK End |
|  | Design Of Area Efficient And Low Power 4-Bit Multiplier Based On Full- swing GDI technique | 2019 | BACK End |
|  | Multistage Linear Feedback Shift Register Counters With Reduced Decoding Logic in 130-nm CMOS for Large-Scale Array Applications | 2019 | BACK End |
|  | Low-Power Near-Threshold 10T SRAM Bit Cells With Enhanced Data-Independent Read Port Leakage for Array Augmentation in 32-nm CMOS | 2019 | BACK End |
|  | Column selection enabled 10 T SRAM utilizing shared diff VDD WRITE and dropped VDD read for FFT on real data. | 2019 | BACK End |
|  | Cell-state-distribution –assisted threshold voltage detector for NAND flash memory | 2019 | BACK End |
|  | Efficient VLSI Implementation of a Sequential Finite Field Multiplier Using Reordered Normal Basis in Domino Logic | 2019 | BACK End |
|  | An Approach to LUT Based Multiplier for Short Word Length DSP Systems | 2018 | Frontend |
|  | Novel High speed Vedic Multiplier proposal incorporating Adder based on Quaternary Signed Digit number system | 2018 | Frontend |
|  | FPGA Implementation of an Improved Watchdog Timer for Safety-critical Applications | 2018 | Frontend |
|  | Unbiased Rounding for HUB Floating-point Addition | 2018 | Frontend |
|  | A Low-Power Yet High-Speed Configurable Adder for Approximate Computing | 2018 | Frontend |
|  | A Low-Power High-Speed Accuracy-Controllable Approximate Multiplier Design | 2018 | Frontend |
|  | The Design and Implementation of Multi – Precision Floating Point Arithmetic Unit Based on FPGA | 2018 | Frontend |
|  | Extending 3-bit Burst Error-Correction Codes With Quadruple Adjacent Error Correction | 2018 | Frontend |
|  | Efficient Modular Adders based on Reversible Circuits | 2018 | Frontend |
|  | MAES: Modified Advanced Encryption Standard for Resource Constraint Environments | 2018 | Frontend |
|  | Chip Design for Turbo Encoder Module for In-Vehicle System | 2018 | Frontend |
|  | Low-Power and Fast Full Adder by Exploring New XOR and XNOR Gates | 2018 | Backend |
|  | Low Power 4×4 Bit Multiplier Design using Dadda Algorithm and Optimized Full Adder | 2018 | Backend |
|  | Low Leakage Fully Half-Select-Free Robust SRAM Cells with BTI Reliability Analysis | 2018 | Backend |
|  | Improved 64-bit Radix-16 Booth Multiplier Based on Partial Product Array Height Reduction | 2017 | Frontend |
|  | Clock-Gating of Streaming Applications for Energy Efficient Implementations on FPGAs | 2017 | Frontend |
|  | An Improved DCM-Based Tunable True Random Number Generator for Xilinx FPGA | 2017 | Frontend |
|  | RoBA Multiplier: A Rounding-Based Approximate Multiplier for High-Speed yet Energy-Efficient Digital Signal Processing | 2017 | Frontend |
|  | DLAU: A Scalable Deep Learning Accelerator Unit on FPGA | 2017 | Frontend |
|  | Overloaded CDMA Crossbar for Network-On-Chip | 2017 | Frontend |
|  | Design of Power and Area Efficient Approximate Multipliers | 2017 | Frontend |
|  | Scalable Approach for Power Droop Reduction During Scan-Based Logic BIST | 2017 | Frontend |
|  | Design of Low-Power High-Performance 2-4 and 4-16 Mixed-Logic Line Decoders. | 2017 | Backend |
|  | Performance Analysis of a Low-Power High-Speed Hybrid 1-bit Full Adder Circuit | 2017 | Backend |
|  | 12T Memory Cell for Aerospace Applications in Nano scale CMOS Technology | 2017 | Backend |
|  | Pre-Encoded Multipliers Based on Non-Redundant Radix-4 Signed-Digit Encoding | 2016 | Frontend |
|  | Flexible DSP Accelerator Architecture Exploiting Carry-Save Arithmetic | 2016 | Frontend |
|  | Low-Cost High-Performance VLSI Architecture for Montgomery Modular Multiplication | 2016 | Frontend |
|  | A High-Speed FPGA Implementation of an RSD-Based ECC Processor | 2016 | Frontend |
|  | Hybrid LUT/Multiplexer FPGA Logic Architectures | 2016 | Frontend |
|  | In-Field Test for Permanent Faults in FIFO Buffers of NOC Routers | 2016 | Frontend |